Amendments to the Specification

Please replace the paragraph beginning at page 4, line 20, with the following amended paragraph:

Prior to shipping a non-volatile memory cell product, a manufacturer will generally test the cells to guarantee that a each bit has ~~a~~ good margin, and that the bit will maintain its programmed or erased state over the lifetime of the cell. The "margin" is the voltage required on a cell's control gate to cause a change in the state of a bit of memory. As illustrated in Figure 2, since a programmable cell has two threshold voltages, it will have two margin voltages: One for the programmed state and one for the erased state. In an EEPROM cell, an erased bit will have a lower margin voltage, typically between about -5V to 0V, and a programmed bit will typically have a higher margin voltage, typically between about 3V and 8V.

Please replace the paragraph beginning at page 18, line 16, with the following amended paragraph:

The structure of Fig. 4H is produced by removing the photoresist used during the most recent etch step. This leaves a region of bare silicon 355 within the gate oxide region 340 on substrate 211 overlying at least a portion of the MD 335. Note that the region 355 may extend into the field oxide region 229. Then, as shown in Figure 4I ~~5E~~, a tunnel oxide layer 358 is grown over the slot of bare silicon surface 355 created by the etch. A tunnel oxide 358 is generated by thermal oxidation at about 850 to 950 °C for about 7 minutes in a dry O_2/Cl atmosphere so that the bare silicon surface in the slot 355 is converted to an oxide layer of about 70 to 100 Å in thickness. This thermal oxidation will further increase the thickness of the gate oxide layer to about 160 to 200 Å over the MD region 335, and about 145 to 190 Å over the well 221.

Please replace the two paragraphs beginning at page 24, line 9, with the following amended paragraphs:

The sense amp, represented by block 708 in Figures 7 and 8, is composed of an n-channel transistor 930 and a p-channel transistor 940, and their associated features depicted ~~within the phantom lines 925~~ in the specific embodiment depicted in Figure 9. The gate 942 of the p-channel transistor 940 is connected to a reference voltage by line 945, and the p-channel source 944 is set to V_{CC}. The n-channel transistor gate 940 is connected to the drain line 706. Output node 709 provides the sense amp output. The circuit 900 is completed by the connection of the n-channel transistor 930 to ground 714 and back to the cell 702 through source line 712.

In a conventional circuit design, the n-channel transistor 930 of the sense amp has its gate 932 connected the drain line 706 ~~934~~. As the cell 702 is turned on by raising the control gate 704 voltage, the current flowing through the cell 702 to the source line 712, which is grounded, pulls drain line node 706 voltage down. As it does so, the n-channel 930 will slowly be turned off because its gate voltage will reach the threshold voltage of that device. The voltage at output node 709 will start rising, pulled up by the p-channel transistor source 944, as the n-channel transistor 930 is turned off; that is, as the voltage at drain line node 706 goes down. Therefore, when the output node 709 voltage increases to the p-channel transistor source 944 voltage, typically V_{CC}, it will be sensing that the cell 702 has turned on. The voltage on the control gate 704 at that moment is called the margin voltage.

Please replace the paragraph beginning at page 31, line 2, with the following amended paragraph:

Those of skill in the art will recognize that the described aspects of the invention may be used alone or in combination to achieve the desired result, namely an erase margin voltage at a testable level in a single poly EEPROM cell. While the present invention is applicable to EEPROM cells generally, it is particularly well-adapted to use with dual row line EEPROM cells which may be biased to provide a testable erase margin voltage without increasing the stress on the cell's the tunnel window. Increased stress is undesirable for data retention and long term cell reliability. Stress-reducing biasing may be achieved by increasing the voltage on a cell's write column (on one side of the tunnel oxide) together with the voltage on the cell's control gate (on the ~~ethe~~ other side of the tunnel oxide), so that the voltage across the cell's tunnel window is not increased along with the margin voltage. This biasing scheme is the subject of patent application Serial No. 08/995,970 ~~(attorney docket No. ALTRP027)~~, entitled BIASING SCHEME FOR REDUCING STRESS IN EEPROM CELLS, filed concurrently herewith and incorporated by reference in its entirety herein for all purposes.